Amendments to the Claims:

1. (withdrawn) A method for manufacturing a block alterable memory cell, such method comprises the following steps:

depositing a screen oxide over a substrate layer;

depositing a mask implant layer over the screen oxide layer;

implanting memory cells in the portion of the substrate layer not covered by the mask implant layer;

etching a screen oxide and an initial gate oxide from memory cells;

depositing tunnel window mask;

etching a tunnel oxide layer;

depositing control poly layer; and

implanting source and drain regions.

2. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein the step of deposing a control poly layer further comprising:

depositing a first oxide layer;

depositing an inter poly layer;

depositing a second oxide layer.

3. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein said tunnel oxide layer having a thickness of 50-70 angstroms.

4. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein said screen oxide layer having a thickness of 200-350 angstroms.

5. (currently amended) A block alterable memory cell, comprising:

a substrate layer having a source implant region, a buried implant region essentially contiguous with said source implant region, a tunnel diode window region within said buried implant region, an active region, a floating gate transistor region essentially contiguous with said active region, and a drain implant region;

a tunnel oxide layer overlaying a portion of said ~~substrate layer~~buried implant region;

a floating gate oxide layer overlaying said floating gate transistor region exclusive of said tunnel diode window region;

a first layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an ~~inter poly~~ interpoly layer overlaying said first layer and said active region, said interpoly layer extending continuously from an edge of said source implant region to an edge of said drain implant region; and

a second layer extending continuously over said floating gate transistor region and said active region, said second layer extending from an edge of said source implant region to an edge of said drain implant region.

6. (previously presented) The block alterable memory cell of claim 5, wherein said substrate layer is a p-type doped substrate.

7. (currently amended) The block alterable memory cell of claim 5, wherein said source implant region, said drain implant region, and said ~~floating gate transistor~~ buried implant region are n-type implants.

8. (currently amended) The block alterable memory cell of claim 5, wherein said first layer and said second layer ~~is~~ are polysilicon ~~and said second layer is oxide~~.

9. (currently amended) The block alterable memory cell of claim 5, wherein said ~~inter poly~~interpoly layer is a nitride layer.

10. (canceled) The block alterable memory cell of claim 5, wherein said substrate layer further comprises a thin surface layer.

11. (currently amended) A semiconductor memory device, comprising:

a memory array arranged into a plurality of rows and a plurality of columns, said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell having a substrate layer with a source implant region, an active region, a floating gate transistor region, a drain implant region, a tunnel oxide layer overlaying a portion of said substrate layer, a first layer overlaying said tunnel oxide layer, an ~~inter poly~~interpoly layer overlaying said first layer, and a second layer extending over said floating gate transistor region and said active region to an edge of said drain implant region;

an input/output port in communication with said memory array; and

a controller coupled to said input/output port and said memory array.

12. (currently amended) The block alterable memory cell of claim 5, wherein said ~~inter poly~~interpoly layer is an ONO layer.

13. (currently amended) A block alterable memory cell, comprising:

a substrate layer having a source doped region, a buried doped region essentially contiguous with said source doped region, a tunnel diode window region within said buried doped region, an active region, a floating gate transistor region essentially contiguous with said active region, and a drain doped region;

a tunnel oxide layer overlaying a portion of said buried doped region ~~substrate layer~~;

a floating gate oxide layer overlaying said floating gate transistor region exclusive of said tunnel diode window region;

a first layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an ~~inter poly~~ interpoly layer overlaying said first layer and said active region, said interpoly layer extending continuously from an edge of said source doped region to an edge of said drain doped region; and

a second layer extending continuously over said floating gate transistor region and said active region, said second layer extending from an edge of said source doped region to an edge of said drain doped region.

14. (previously presented) The block alterable memory cell of claim 13, wherein said substrate layer is a p-type doped substrate.

15. (currently amended) The block alterable memory cell of claim 13, wherein said source doped region, said drain doped region, and said ~~floating gate transistor~~buried doped region have n-type dopants.

16. (currently amended) The block alterable memory cell of claim 13, wherein said first layer and said second layer ~~is~~ are polysilicon ~~and said second layer is oxide~~.

17. (currently amended) The block alterable memory cell of claim 13, wherein said ~~inter poly~~interpoly layer is a nitride layer.

18. (currently amended) The block alterable memory cell of claim 13, wherein said ~~inter poly~~interpoly layer is an ONO layer.

19. (canceled) The block alterable memory cell of claim 13, wherein said substrate layer further comprises a thin surface layer.

20. (currently amended) A semiconductor memory device, comprising:

memory array arranged into a plurality of rows and a plurality of columns, said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell having a substrate layer with a source doped region, an active region, a floating gate transistor region, a drain doped region, a tunnel oxide layer overlaying a portion of said substrate layer, a first layer overlaying said tunnel oxide layer, an ~~inter poly~~ interpoly layer overlaying said first layer, and a second layer extending over said floating gate transistor region and said active region to an edge of said drain doped region;

an input/output port in communication with said memory array; and

a controller coupled to said input/output port and said memory array.

21. (currently amended) A semiconductor memory device, comprising:

a memory array arranged into a plurality of rows and a plurality of columns, said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell having a substrate layer with a source doped region, an active region, a floating gate transistor region, a drain doped region, a tunnel oxide layer overlaying a portion of said substrate layer, a first layer overlaying said tunnel oxide layer, an ~~inter poly~~interpoly layer overlaying said first layer, and a second layer extending over said floating gate transistor region and said active region to an edge of said drain doped region; and

an input/output port in communication with said memory array.

22. (new) An abutting pair of block alterable memory cells, each memory cell comprising:

a substrate layer having a source implant region, a buried implant region essentially contiguous with said source implant region, a tunnel diode window region within said buried implant region, an active region, a floating gate transistor region essentially contiguous with said active region, and a drain implant region;

a tunnel oxide layer overlaying a portion of said buried implant region;

a floating gate oxide layer overlaying said floating gate transistor region exclusive of said tunnel diode window region;

a first layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an end tour poly layer overlaying said first layer and said active region, said interpoly layer extending continuously on from an edge of said source implant region to an edge of said drain implant region; and

a second layer extending continuously on over said floating gate transistor region and said active region, said second layer extending from an edge of said source implant region to an edge of said drain implant region.

23. (new) The abutting pair of block alterable memory cells of claim 22, wherein each of said pair of abutting block alterable memory cells is coupled essentially contiguous at said source implant region.

24. (new) An abutting pair of block alterable memory cells, each memory cell comprising:

a substrate layer having a source doped region, a buried doped region essentially contiguous with said source doped region, a tunnel diode window region within said buried doped region, an active region, a floating gate transistor region essentially contiguous with said active region, and a drain doped region;

a tunnel oxide layer overlaying a portion of said buried doped region;

a floating gate oxide layer overlaying said floating gate transistor region exclusive of said tunnel diode window region;

a first layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an end tour poly layer overlaying said first layer and said active region, said interpoly layer extending continuously on from an edge of said source doped region to an edge of said drain doped region; and

a second layer extending continuously on to over said floating gate transistor region and said active region, said second layer extending from an edge of said source doped region to an edge of said drain doped region.

25. (new) The abutting pair of block alterable memory cells of claim 24, wherein each of said pair of abutting block alterable memory cells is coupled essentially contiguous at said source doped region.